Robust black start of an offshore wind farm with DRU based HVDC link using power synchronization control

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***Abstract*—This paper introduces a universal power synchronization controller for grid-side control of the wind turbine conversion systems in an offshore wind farm with a diode rectifier in the offshore substation of the HVDC link. The controller incorporates voltage-power droop controllers in the outer loop to enable the operation of this setup. To effectively handle the impact of large delays during black start and power ramp phases, virtual active and reactive power quantities are defined. These quantities are computed based on the current references prior to any modifications that might be needed to meet converter current and voltage limits or source constraints. Utilizing them in the outer loop ensures a balanced power sharing and a stable operation whenever the original (unmodified) current references are not realized. Case studies confirm the robustness of the proposed controller.**

***Index Terms*—grid-forming control, wind-generator systems, power synchronization**

I. Introduction

Among renewable energy sources, the global capacity of offshore wind farms (OWFs) has been rapidly increasing thanks to substantial investments and recent technological advancements. An OWF with a diode rectifier unit (DRU) based HVDC link connection offers several advantages over the one with a traditional voltage source converter-based HVDC link connection. These advantages include the reduced offshore substation complexity, reduced size and price as well as the increased reliability and efficiency. Consequently, there has been significant interest in research for such OWFs. The EU-funded project PROMOTioN[1] delivered a proof of concept for the operation of a DRU-based HVDC link in combination with grid-forming wind converters. More recently, advanced grid-forming concepts for a similar setup have been developed within the FlexH_2 project[2], in which ABB is contributing. This project aims to design a novel OWF that also incorporates an onshore hydrogen production.

Grid-forming control is becoming essential for the stable and reliable operation of modern power systems, particularly as we integrate more renewable energy sources with power electronic interfaces. This control strategy is characterized by its ability to support islanded operation, enabling converters to establish and regulate both voltage and frequency. In OWFs with a DRU-based HVDC link connection, as considered in this work, grid-forming control is not only desirable but also indispensable for the grid-side control of wind turbine (WT) converters. This necessity arises from the fact that a DRU cannot form the voltage and lacks the ability to control power flow actively.

In order to enable this type of OWF configuration, several grid-forming control proposals have been made for the grid-side control of WT converters [1]–[8]. Among these works, many, such as [1]–[4], rely on reactive power synchronization (or Qf-droop), motivated also by the dynamics of the large capacitor bank for reactive power compensation. The authors in [7] introduced an additional coupling from active power to angle via the so-called angle feedforward control to better dampen oscillations observed between the WTs. As an alternative, [8] employs a QV droop with additional couplings from frequency to voltage magnitude, and from active power to angle in a phase-locked loop (PLL)-based scheme, again better mitigating reactive power swings among WTs.

In contrast to these existing works, our control design utilizes the universal framework proposed in [9]. This architecture integrates the well-established (active) power synchronization control (PSC) from [10] into vector current control (VCC) that has inherent current limiting capability. It also offers greater flexibility with a point-of-common-coupling (PCC) voltage alignment of the voltage and power references. Additionally, it ensures a smooth transition from more conventional converter control schemes, e.g., those using a PLL, and it is compatible with the generic PLL-based framework of [11]. This paper introduces the necessary voltage control modifications that enable the use of universal PSC (UPSC) in the DRU-based OWF setup.

Despite these modifications, the main challenges associated with grid-forming control, stemming from the limited capabilities of the converter and the source, persist. Significant

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communication delays between WTs during black starts can cause converters to hit their current or modulation limits. Similarly, a delayed power ramp might necessitate power absorption from some WTs to remain synchronized, which may not be desirable or even feasible for the WT conversion systems. Deviating from the original current reference can lead to a loss of synchronism with the grid, characterized by unstable frequency and/or voltage dynamics. This paper develops virtual active and reactive power-based control loops to address this issue. These virtual power quantities are calculated using the alternating voltage controller's current references rather than the actual current measurements, ensuring that the outer loops remain unaffected by any subsequent changes to the current references. Virtual active power for the synchronization loop has already been presented by [12], [13]. During fault clearances and phase jumps, these works have shown that using it can improve large signal stability of the synchronization loop. For the UPSC under consideration, we will demonstrate that both virtual active power and virtual reactive power are essential to enable flawless black start and power ramp stages in OWFs.

Our contributions are as follows. We introduce a UPSC scheme with voltage-power droop controllers in the outer loop to enable its use in OWFs with DRU-based HVDC link. This controller provides a direct coupling between active power and the voltage magnitude. To circumvent stability issues associated with delays in black start and power ramp stages, we introduce virtual active and virtual reactive power. To the best of our knowledge, this is the first publication to employ virtual power quantities within voltage-power droop controllers and also to demonstrate their advantages. Moreover, it is the first publication to highlight the specific benefits of virtual reactive power. Case studies are presented to showcase the performance of the proposed control scheme.

Notation: Complex space vectors in the (synchronous) dq-frame are denoted by boldface letters, e.g., $\mathbf{i}$. When they refer to the (stationary) $\alpha\beta$-frame, the superscript ^{s} is added, $\mathbf{i}^s$. Real transfer functions that map between complex space vector spaces—implying no cross-coupling between the two components—are denoted by italic letters, e.g., $G(s)$. Here, the Laplace variable s is to be interpreted as the derivative operator $s = \frac{d}{dt}$, where appropriate. In the remainder, all quantities (including frequency and time—except in the simulations) are normalized. A first-order low pass filter is denoted by $H_\alpha(s) = \frac{\alpha}{s+\alpha}$, and α is referred to as its bandwidth. The superscript * denotes the (Hermitian) conjugate.

II. Preliminaries and System Configuration

A. OWF configuration

In Figure 1, an OWF, consisting of multiple strings, is connected to the onshore grid via an HVDC link using a 24-pulse DRU on the offshore side. Optionally, a reactive power compensation unit and/or harmonic filters can be available at the offshore bus, denoted by voltage $\mathbf{v}^s_{\text{off}}$. The controlled current source depicted at the onshore side of the HVDC link approximates the onshore converter. This current source controls v_{on}, the DC voltage of the HVDC link at the onshore side, using a PI controller and a feedforward. In simulations, this source is restricted from energizing the HVDC link to ensure that the black start stage is entirely managed by the WTs.

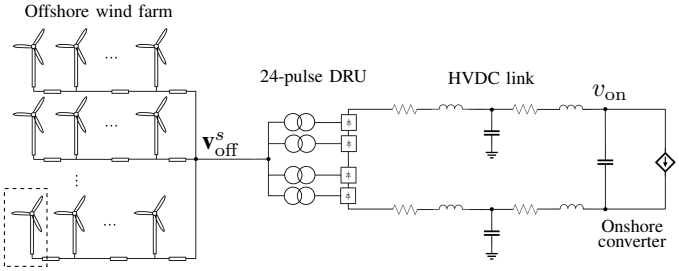

Fig. 1: OWF with a DRU-based HVDC link.

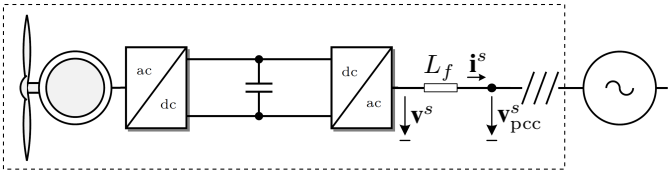

Fig. 2: Example circuit for the WT conversion system.

B. Wind converter system

Figure 2 illustrates the circuit of the medium-voltage (MV) WT conversion system and the related notation. The conversion system comprises a dual conversion line, as the permanent magnet synchronous generator has two sets of three-phase windings. In the interest of space, the intricacies of this dual conversion setup are not presented; see [14] for further details. On the converter-side of the PCC, we have the stray-inductance of the transformer, L_f. The resistances are small, and they are not presented, as their inclusion in the control scheme is trivial. A stiff voltage is illustrated here for presentation purposes only. The wind turbine generator-side converters, which are not shown explicitly, are primarily responsible for controlling the DC-link voltages of the WT conversion system. The details of the generator-side control scheme are also omitted in the interest of space.

III. Universal Power Synchronization Controller

Several definitions are introduced in the following for the complete UPSC scheme provided in Figure 3. The active and reactive power references are denoted by P_{ref} and Q_{ref}, respectively. The active power reference is provided by the high-level wind turbine controller, while the reactive power reference is communicated by the grid operator. An external voltage magnitude reference V_{ext} could be communicated or generated by other high-level control loops. The term $P_{\min}$ denotes the minimum allowed power to limit the reverse power flow, which is nominally set to 0. The term $I_{\max}$ is the maximum allowed phase current magnitude. Finally, $\boldsymbol{u}$ denotes the switching signal. Other quantities are either defined later or are clear from the context of power conversion control.

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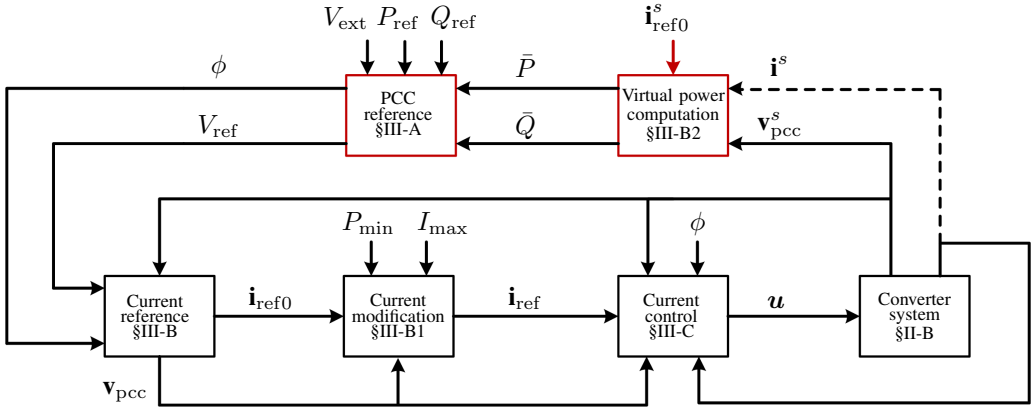

Fig. 3: A high-level block diagram of the complete UPSC scheme for grid-side control of the WT conversion system. The red blocks highlight the modifications for the DRU application compared to [9].

The virtual power computation stage calculates both the active and reactive power, as well as the virtual active and reactive power. The active power is simply $P = \text{Re}\{\mathbf{v}^s_{\text{pcc}}\mathbf{i}^{s*}\}$, whereas the reactive power is $Q = \text{Im}\{\mathbf{v}^s_{\text{pcc}}\mathbf{i}^{s*}\}$. From this stage, the terms $\bar{P}$ and $\bar{Q}$ are passed on to the PCC reference creation stage, and it will select between the virtual power and the actual measurements. The reasoning behind will be explained in the following sections. The PCC reference creation stage includes the synchronization loops and the droop controllers comparing $\bar{P}$ and $\bar{Q}$ with their respective references.

The current reference generation stage calculates the current references that would push the PCC voltage towards its reference. Notice that some blocks have combined features, e.g., the current reference stage calculates also the positive sequence of the PCC voltage, to keep the block diagram simple. The current modification stage is where the limited capabilities of the converter and the source are integrated into the scheme. Finally, the current controller closes the loop for current, and creates the switching signal. For the input admittance analysis of the complete scheme under normal operating conditions, the reader is referred to [15].

A. PCC voltage reference generation

1) Synchronization and the dq*-frame (reference) angle:* The power synchronization loop generates the dq-frame angle ϕ. This angle is also the reference angle for the PCC voltage:

$$\phi = (1/s)\left[\omega_1 + K_P(s)(P_{\text{ref}} - \bar{P})\right], \tag{1}$$

where ω_1 is the nominal synchronous frequency, and $K_P(s) = \frac{sT_d+1}{sM+k_m}$, with T_d being the time constant used for damper winding emulation, k_m being the frequency droop constant, and M being the virtual inertia constant.

2) Voltage magnitude reference: The PCC voltage magnitude reference is generated by

$$\begin{aligned} V_{\text{ref}} = V_{\text{ext}} &+ K_{QV}(s)\left[Q_{\text{ref}} - H_{\alpha_Q}(s)\bar{Q}\right] \\ &+ K_{PV}(s)\left[P_{\text{ref}} - H_{\alpha_P}(s)\bar{P}\right]. \end{aligned} \tag{2}$$

This block includes:

(a) QV control/droop: A QV droop functionality, where $K_{QV}(s) = K_{QV}$ and $\alpha_Q < \omega_1$, is necessary for reactive power sharing in parallel operation [16]. During black start scenarios with communication delays, QV droop synchronizes the voltage magnitude ramps across multiple converters, see Section IV-A.

(b) PV control/droop: A PV control functionality, where $K_{PV}(s) = K_{PV} + \frac{K_{PV,I}}{s}$ and $\alpha_P < \omega_1$, is essential to push power over loads with strong voltage sensitivity, such as DRU. Specifically, the active power flow is proportional to the voltage magnitude (see the models provided in [5], [8]). Thus, this is the primary component that enables the use of UPSC in the DRU-based OWF setup. Moreover, PV droop, the proportional part of PV control, can improve passivity in the low frequency range [15, §IV]. The tuning here must be based on the dynamical requirements set for the OWF. During power ramp scenarios with delays, PV control also ensures a synchronous voltage increase, and thus maintains a balanced reactive power sharing among WTs, see Section IV-B.

B. Current reference generation

The alternating voltage controller (AVC) generates:

$$\mathbf{i}_{\text{ref0}} = \frac{P_{\text{ref}} - jQ_{\text{ref}}}{V_{\text{ref}}} + \frac{1}{R_a}\left(1 + \frac{\alpha_a}{s}\right)\left[V_{\text{ref}} - H_{\alpha_F}(s)\mathbf{v}_{\text{pcc}}\right], \tag{3}$$

where R_a is the proportional gain of the inner current controller, α_a is the integral control bandwidth (generally chosen small $\alpha_a < 0.05\omega_1$), and α_F is the PCC voltage feedforward bandwidth (e.g., $\alpha_F < R_a/L_f$). The first additive term is the reference feedforward proposed in [17], while the second additive term, derived in [9, §III], unifies VCC and PSC. These current references can also be mapped to the $\alpha\beta$-frame as $\mathbf{i}^s_{\text{ref0}}$ using the angle ϕ.

1) Reference modifications: Two critical considerations are listed for the limitations of the converter and the source.

(a) Reverse power limitation: The following equation limits the reverse power flow:

$$\mathbf{i}_{\text{refr}} = \mathbf{i}_{\text{ref0}} - \frac{\mathbf{v}_{\text{pcc},f}}{|\mathbf{v}_{\text{pcc},f}|^2}\min\{0,\ \text{Re}\{\mathbf{v}_{\text{pcc},f}\mathbf{i}^*_{\text{ref0}}\} - P_{\text{min}}\}, \tag{4}$$

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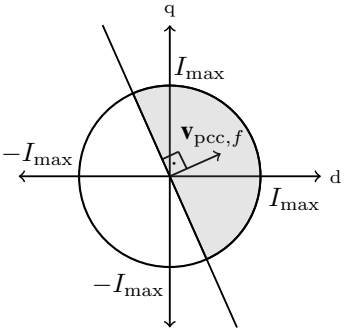

Fig. 4: Example for the current limits when $P_{\min} = 0$. The shaded area represents the safe operating region.

where $\mathbf{v}_{\mathrm{pcc},f} = H_{\alpha_F}(s)\mathbf{v}_{\mathrm{pcc}}$. In essence, if the AVC current reference, $\mathbf{i}_{\mathrm{ref0}}$, would result in a reverse power exceeding the threshold $P_{\min}$, a simple projection step removes the excess while preserving the reactive power component specified by the AVC.

(b) Current magnitude limitation: Converters can generally tolerate a maximum current of approximately 120% of the rated current for extended periods [18]. During transients, however, the AVC may generate a reference that exceeds this limit, denoted as $I_{\max}$. Angle preserving scaling is used for magnitude limitation ensuring that the reverse power limitation is also preserved:

$$\mathbf{i}_{\mathrm{ref}} = \frac{I_{\max}}{\max\{|\mathbf{i}_{\mathrm{refr}}|, I_{\max}\}}\mathbf{i}_{\mathrm{refr}}. \tag{5}$$

Figure 4 illustrates an example constraint set for $P_{\min} = 0$. The two reference modification steps above sequentially constrain the current reference $\mathbf{i}_{\mathrm{ref0}}$ within the safe operating region, which is depicted by the shaded area.

2) Virtual power computation: Whenever any of the modifications above are active, or whenever the current controller itself does not exhibit a good tracking performance (e.g., due to modulation index limits), we face the risk of loss of power sharing or even loss of synchronism. To this end, the virtual active and reactive power terms are defined and calculated based on the unmodified AVC current references:

$$P_{\mathrm{virt}} = \mathrm{Re}\{\mathbf{v}^s_{\mathrm{pcc}}\mathbf{i}^{s*}_{\mathrm{ref0}}\}, \quad Q_{\mathrm{virt}} = \mathrm{Im}\{\mathbf{v}^s_{\mathrm{pcc}}\mathbf{i}^{s*}_{\mathrm{ref0}}\}. \tag{6}$$

For the control scheme presented in the case studies, we replace the measurements with their virtual counterparts, i.e., $\bar{P} = P_{\mathrm{virt}}$ and $\bar{Q} = Q_{\mathrm{virt}}$, and this substitution is active at all times. In other words, the synchronization loop in (1) and the QV and PV controllers in (2) operate exclusively with virtual active and reactive power, ensuring that their behavior remains unaffected by any subsequent changes in the currents. This design choice demonstrates better the effectiveness of virtual power, and emphasizes that no detection mechanism is required to activate the virtual power-based control loops. The corresponding block in Figure 3 still takes the actual current measurements as an optional (dashed) input, allowing for the implementation of a switch-over logic for this selection process if desired.

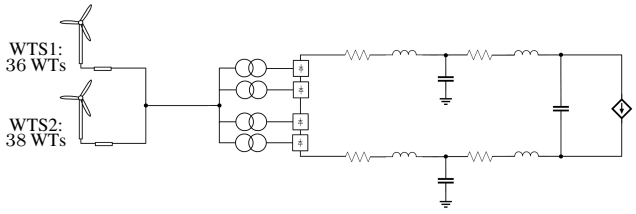

Fig. 5: Simulation environment with string aggregation.

C. Current control design

The control scheme described up to now is compatible with various current controllers. We employ an $\alpha\beta$-frame current controller with a PCC voltage feedforward which also accounts for the voltage drop across the inductance L_f:

$$\mathbf{v}^s_{\mathrm{ref}} = R_a(\mathbf{i}^s_{\mathrm{ref}} - \mathbf{i}^s) + j\omega_1 L_f \mathbf{i}^s_{\mathrm{ref}} + \mathbf{v}^s_{\mathrm{pcc},f}, \tag{7}$$

where R_a is the proportional gain, and $\mathbf{v}^s_{\mathrm{ref}}$ is the reference voltage (e.g., to be created via PWM). For MV applications, model predictive pulse pattern control (MP^{3}C) could be considered essential, since optimized pulse patterns bring in significant advantages, and MP^{3}C maximizes the benefits of them [19]. As a remark, the controller above has been shown to approximate MP^{3}C well, see [14].

IV. Case Studies

We conduct studies in an environment—implemented in MATLAB Simulink—where the dual converter system of [14] is used as an interface for a 19.1 MVA WT generator. The setup, illustrated in Figure 5, consists of two aggregated strings. WTS1, the top string, is an aggregation of 36 WTs, whereas WTS2, the bottom string, is an aggregation of 38 WTs. The relevant system parameters and rated values are given in Table I. Other parameters (e.g., those relating to the cables, diode rectifier, its transformer, and the HVDC link) are considered confidential. The base systems are defined with respect to the aggregations.

The controlled current source on the onshore side regulates the DC voltage with a control and feedforward bandwidth of 25 Hz. As mentioned before, this source is restricted from black starting the HVDC link. The control parameters are detailed in Table II. Since we are interested in system behavior in the low-frequency range, we work with averaged converter models for the WT conversion system. However, the switching and control system delays are taken into account, e.g., by considering the actual sampling intervals and control time scales of our converters. To further simplify the setup, we assume that the reactive power reference is not communicated (i.e., $Q_{\mathrm{ref}} = 0$), and V_{ext} is generated locally, meaning there is no secondary supervisory control. To abide by the page limitations, we present only the most relevant plots.

A. Black start with communication delays

In this case study, we analyze the black start procedure that is performed by the two strings. Their voltage ramps are set to $0.8\,\mathrm{pu}$ with slope $0.6\,\mathrm{pu/s}$. WTS2 receives the voltage ramp

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TABLE I: WT system parameters and rated values.

Parameter	Symbol	Value
Rated apparent power of the transformer	$S_{\mathrm{R,trafo}}$	18 MVA
Rated voltage at the primary (grid)	$V_{\mathrm{R,prim}}$	66 kV
Rated voltage at the secondary (converter)	$V_{\mathrm{R,sec}}$	3.1 kV
Rated angular frequency	ω_1	$2\pi 50\,\mathrm{rad\,s^{-1}}$
Filtering inductance equivalent for trafo	L_f	0.18 pu
Filtering resistance equivalent for trafo	R_f	0.01 pu
DC-link voltage of WT	V_{dc}	1.9754 pu

TABLE II: Control parameters in per unit.

Parameter/Symbol	Value	Parameter/Symbol	Value
H (Inertia time const.)	1 s	R_a	0.36 pu
k_m	20 pu	α_a	0.01 pu
T_d	0 pu	α_F	2 pu
K_{QV}	0.05 pu	$I_{\max}$	1.2 pu
α_Q	0.2 pu	K_{PV}	0.75 pu
α_P	0.5 pu	$K_{PV,I}$	5 pu

start signal with a communication delay of 300 ms, which is large compared to typical communication delays in this setup, e.g., 50 to 100 ms. Whenever virtual power is disabled for a control loop, it means that the actual power measurements are used instead.

1) Virtual power disabled only in QV and PV control, but enabled in the synchronization loop: Figure 6 illustrates the loss of synchronism that occurs when WTS2 joins the black start late, and if the QV and PV control loops do not utilize virtual power. This happens because both strings reach their current and reverse power limits due to the delay between the voltage ramps. The voltage-power control loops attempt to correct this while being unaware of the limits. Similar observations can be made if one of the virtual powers in the QV or PV control is disabled.

2) Virtual power enabled in all controllers: Figure 7 showcases the flawless black start under excessive communication delays despite having no secondary supervisory control. One can observe the time instances where we benefit from having virtual power-based control loops especially from the difference between the virtual reactive power and the reactive power measurements in the plots.

B. Delayed power ramps

Once the black start is completed, the two strings enter the power ramp stage. In this scenario, WTS2 ramps with a delay of 1 s, when compared to WTS1.

1) Virtual power disabled in all control loops and the limit $P_{\min} = -\infty$: Figure 8 illustrates that when reverse power limits are removed, the use of virtual power is no longer necessary to handle delayed power ramps. The PV control successfully achieves a synchronous voltage increase, which can be confirmed from the balanced reactive power sharing.

2) Virtual power disabled only in PV control and the limit $P_{\min} = 0$: Figure 9 demonstrates that the absence of virtual power in PV control alone can prevent the power ramp. During asynchronous power ramps, it is imperative for WTS1 and WTS2 to increase voltage synchronously. Failure to do so results in a large reactive power transfer from WTS1 to

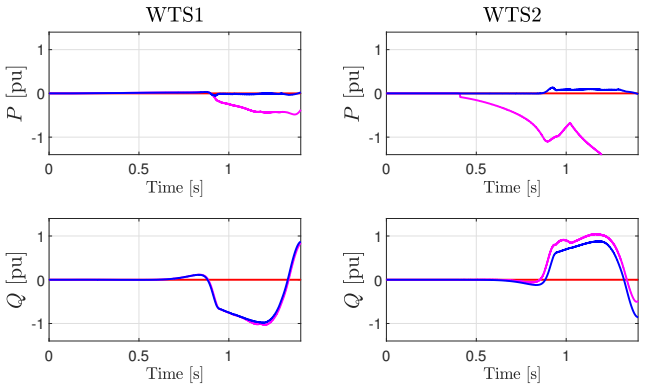

Fig. 6: Delayed black start: Virtual power disabled. *(Red: Reference. Blue: Measurement. Purple: Virtual)*

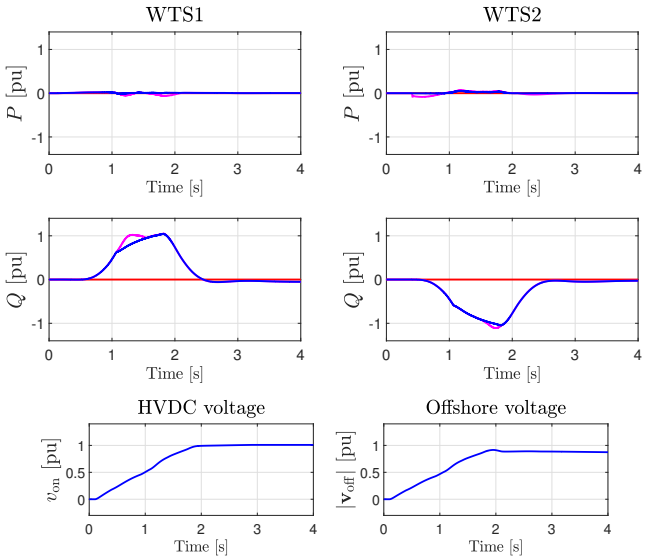

Fig. 7: Delayed black start: Virtual power enabled.

WTS2, causing WTS1 to reach its current limits. Observations related to loss of synchronism can be made if instead the virtual power in power synchronization loop is disabled.

3) All virtual powers enabled and with $P_{\min} = 0$: Figure 10 showcases the flawless power ramp. The virtual reverse power absorbed by WTS2 ensures synchronous voltage increase whenever necessary.

V. Conclusion

We presented a UPSC scheme that enables flawless black start and power ramp stages in OWFs with a DRU based HVDC link connection. To achieve this, a voltage magnitude reference was generated by QV and PV voltage-power droop controllers. To address the stability issues arising from the limited capabilities of the converter and the source, active and reactive power measurements were replaced by their virtual counterparts using the original (unmodified) current references generated by the AVC.

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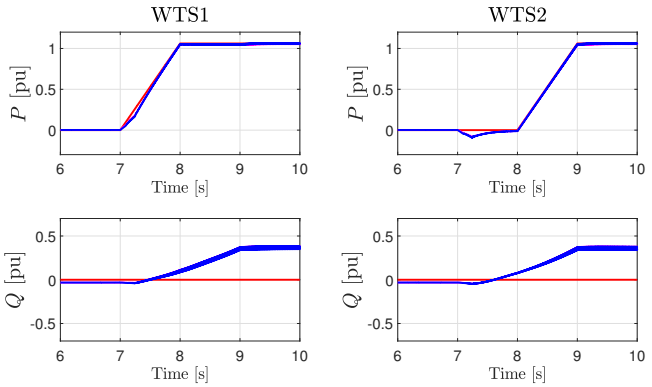

Fig. 8: Delayed ramp: Virtual power disabled and $P_{\min} = -\infty$.

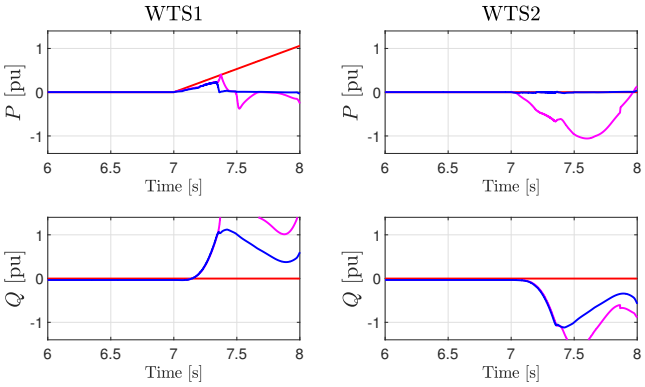

Fig. 9: Delayed ramp: Virtual power disabled and $P_{\min} = 0$.

To the best of our knowledge, this is the first publication to employ virtual power quantities within QV and PV control loops and also to demonstrate the advantages to do so. Moreover, it is the first publication to highlight the specific benefits of virtual reactive power. Case studies confirmed the improved robustness of the controller for the DRU-based OWF setups considered in the FlexH$_2$ project.

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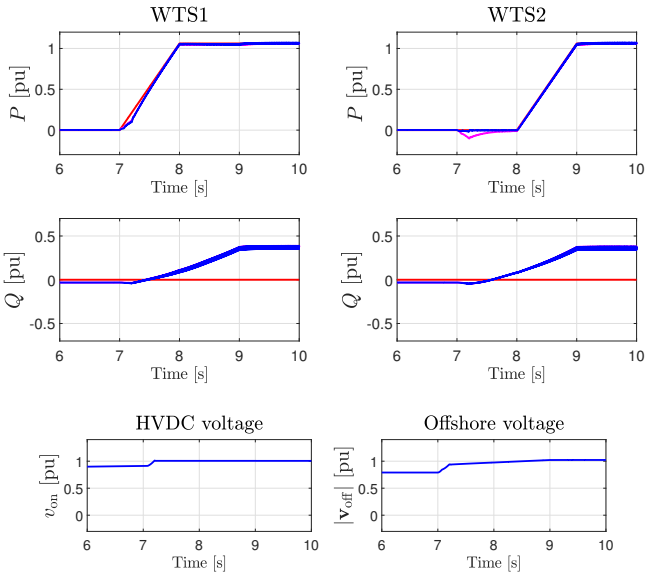

Fig. 10: Delayed ramp: Virtual power enabled and $P_{\min} = 0$.

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